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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/673,677 | 09/30/2003 | Jared LeVan Zerbe | 57941.000013 | 2037 |

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| EXAMINER | |
|---|---|
| LEE, SIU M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2611 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
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| 3 MONTHS | 01/24/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/673,677 | ZERBE ET AL. | |
| | Examiner | Art Unit | |
| | Siu M. Lee | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *9/30/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *31-55* is/are allowed.

6)☒ Claim(s) *17-20,23 and 26* is/are rejected.

7)☒ Claim(s) *1-16,21,22,24,25 and 27-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/29/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claim1 is objected to because of the following informalities:

Please define PAM, MSB and LSB where first mentioned in claim 1.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 18 and 26-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(1) Claim 18 recites the limitation "differential offset signal" in line 2. There is insufficient antecedent basis for this limitation in the claim.

(2) Claim 26 recites the limitation "the plurality of pairs of unbalanced input transistors" in lines 15-16. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang in view of Gorecki et al. (US 2003/0194016 A1).

Zhang discloses a data processing circuit that comprising a first pair of differential input transistors configured to receive a differential input signal (differential pair of transistors 701 and 702 in figure 7, column 6, lines 33-35); a second pair of differential input transistors (second differential pair of transistor 705 and 706 in figure 7, column 6,lines 32-33), coupled to the pair of input transistors (the second pair of transistor coupled to the output of the first differential pair 701-702 in figure 7, column 6, lines 36-37), and configured to receive a differential equalization signal (transistor pair 705 and 706 are differential pair transistor, column6, lines 32-33); a linear load coupled to the first pair of transistors and the second pair of transistors (load resistor 721 in figure 7, column 6, lines 42-43); and a pair of current sources coupled to the pair of input transistors and the pair of equalization transistors (current source 750 and 751 in figure 7, column 6, lines 40).

Zhang fails to disclose to receive of a multi-PAM input signal.

However, Gorecki et al. discloses a PAM-4 decoder module 922 perform operation associated with the decoding of symbol using PAM-4 coding technique (paragraph 0060, lines 1-4).

It is desirable to use a multi-level PAM signal because it can encode a plurality of bit data onto a signal (paragraph 0006, lines 1-10). Therefore, it would have been

obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Gorecki et al. in the circuit of Zhang to improve the transfer rate of the circuit.

3. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaussi et al. (US 6,825,696 B2) in view of Gorecki et al. (US 2003/0194016 A1).

(1) Regarding claim 19:

Jaussi et al. discloses a circuit comprising a pair of input transistors configured to receive a differential input signal (differential pairs 126 with the transistor pair 130 and 131 in figure 1C, which is located in the differential amplifier 106 of figure 1A, column 2, lines 49-54); a pair of transistors, coupled to the pair of input transistors (differential pair 128 with the transistors 132 and 133 in figure 1C, which is located in the differential amplifier 106 of figure 1A, column 2, lines 49-54), and configured to receive a differential signal; a nonlinear load coupled to the pair of input transistors and the pair of equalization transistors (non-linear load 116 in figure 1A, column 3, lines 27-31); and a pair of switches coupled to the pair of input transistors and the pair of equalization transistors (switch 164 and 166 in figure 1A, column 5, lines 36-56).

Jaussi et al. fails to disclose to receive of a multi-PAM input signal.

However, Gorecki et al. discloses a PAM-4 decoder module 922 perform operation associated with the decoding of symbol using PAM-4 coding technique (paragraph 0060, lines 1-4).

It is desirable to use a multi-level PAM signal because it can encode a plurality of bit data onto a signal (paragraph 0006, lines 1-10). Therefore, it would have been

obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Gorecki et al. in the circuit of Zhang to improve the transfer rate of the circuit.

(2) Regarding claim 20:

Jaussi et al. further discloses a circuit wherein the pair of switches are clocked at a sampling rate (switch 164 and 166 are clocked with a clock signal in figure 1).

4. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al. (US 6,462,623 B1) in view of Gorecki et al. (US 2003/0194016 A1).

Horan et al. discloses a circuit comprising first and second pairs of input transistors configured to receive a differential input signal (the circuit in figure 4C comprises of plurality of inverter and the detail of each inverter is explained in figure 5A, each inverter comprises a pair of differential input transistors (510A and 510B in figure 5A) that receives differential input signal, IN_N and IN_P, column 9, lines 60-63); first and second pairs of adjustable resistive elements, coupled to the first and second pairs of input transistors, respectively (in each inverter ,a pair of variable resistor R1 and R2 is couple to the transistor pair 510A and 510B in figure 5A, column 10, lines 6-7), and configured to receive a differential control signal (Vina and Vinb in figure 5A); a load coupled to the first and second pairs of input transistors (load capacitor 506A and 506B in figure 5A, column 9, lines 55-56); and a pair of current sources coupled to the first and second pairs of adjustable resistive elements, respectively (each inverter has a voltage source couple to the 520 couple to the adjustable resistive element R1 and R2 in figure 5A, column 9, lines 63-66).

Horan et al. fails to disclose to receive of a multi-PAM input signal.

However, Gorecki et al. discloses a PAM-4 decoder module 922 perform operation associated with the decoding of symbol using PAM-4 coding technique (paragraph 0060, lines 1-4).

It is desirable to use a multi-level PAM signal because it can encode a plurality of bit data onto a signal (paragraph 0006, lines 1-10). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Gorecki et al. in the circuit of Zhang to improve the transfer rate of the circuit.

***Allowable Subject Matter***

5. Claims 1-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten to overcome the objection in claim 1.

Claims 18, 21-22, 24-25, 27-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 31-55 are allow.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Werner et al. (US 2002/0091948 A1) discloses an apparatus and method for improving resolution of a current mode driver. Jaussi et al. (US 2004/0119627 A1) discloses a pulse amplitude-modulated signal processing. Zerbe

(US 6396329 B1) discloses a method and apparatus for receiving high speed signals with low latency.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M. Lee
1/11/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER